

In the Specification

Please amend paragraph 0014 as follows:

[0014] FIG. 3 is a perspective view of an example semiconductor device and FIG. 4 is a cross-sectional view taken along a line of A-A' of FIG. 3. As shown in FIGS. 3 and 4, an example semiconductor device includes a capacitor having a bottom electrode, a dielectric layer and an upper electrode, successively formed on a semiconductor substrate 110. A first insulating layer 102 is formed on the semiconductor substrate 110 to cover the upper electrode 100c. A plurality of via holes exposing the bottom and upper electrodes are formed on a certain portion of the first insulating layer and first contact plugs 104a are formed by filling the plurality of via holes with metal material.

Please amend paragraph 0016 as follows:

[0016] A second insulating layer 106 is formed on the semiconductor substrate 110 to cover the first metal wiring 104 and the second contact plug 108a. A plurality of via holes exposing the second contact plugs 108a are formed on a certain portion of the second insulating layer 106 and anti-fuse 108c is formed in a certain thickness in each via hole. A third contact plug 108b is formed on the anti-fuse, which serves to vary the capacitance. A second metal wiring 108 electrically connected to the third contact plug 108b is formed on the second insulating layer covering the third contact plug 108b.

Please amend paragraph 0019 as follows:

[0019] Then, a first insulating layer 102 is formed on the semiconductor substrate 110 including the upper electrode 100c. Successively, a photoresist (not shown) is coated on the first insulating layer 102, and the first insulating layer 102 is selectively etched and removed by a conventional photolithography process and an etching process. As a result, a first via hole 103 exposing the surfaces of the bottom and upper electrodes, is formed by the selective etching of the first insulating layer 102.

Please amend paragraph 0023 as follows:

[0023] In a state that the second via hole 107 has been formed, as shown in FIG. 5D, a metal layer, i.e., a first metal layer for forming an anti-fuse is formed in a certain thickness on the semiconductor substrate 110 including in the second via hole 107. Then, a conductive metal layer, i.e., a second metal layer is formed on the semiconductor substrate 110 including the first metal layer to sufficiently fill the second via hole. Then, the first metal layer and second metal layer are planarized with the second insulating layer 106. Thus, the anti-fuse 108c is formed in the second via hole 107 and a third contact plug 108b is formed inside the anti-fuse.